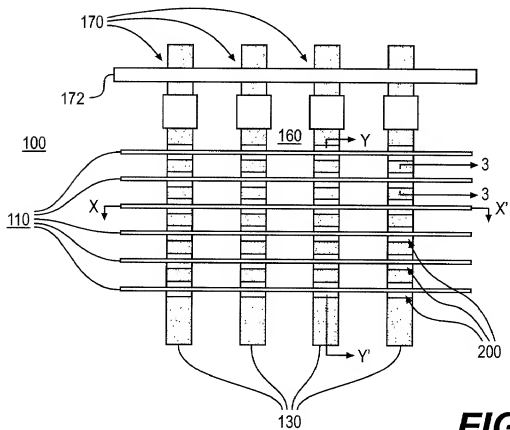
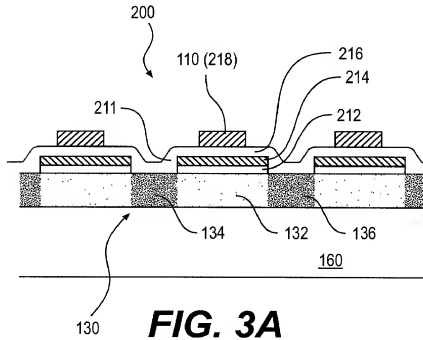


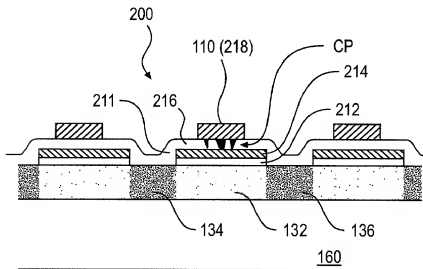
FIG. 10 is a block diagram of a memory device. The device includes an ADDRESS DECODER (120) connected to ROW ADDRESSES (110). A central memory array (100) is connected to the decoder and a MULTIPLEXER (140). The MULTIPLEXER (140) is connected to DATA ADDRESSES (130) and an I/O block (150).



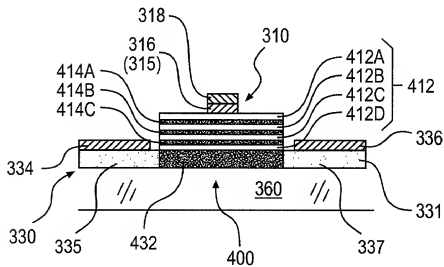
**FIG. 2**



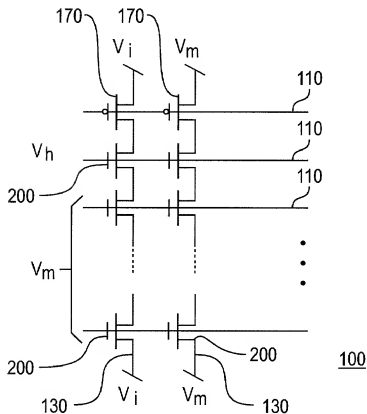
**FIG. 3A**



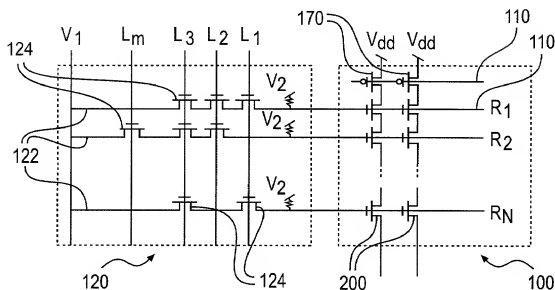
**FIG. 3B**



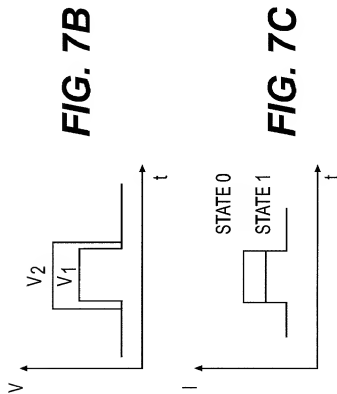
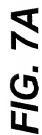
**FIG. 5**

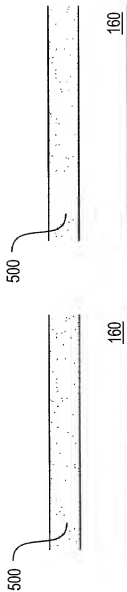


**FIG. 6**

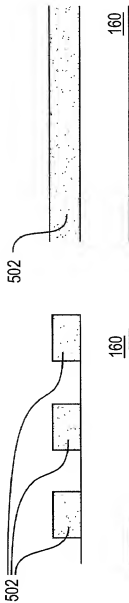


**FIG. 8**

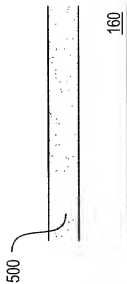




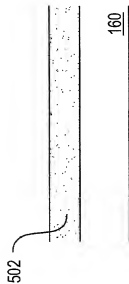
**FIG. 9A**



**FIG. 10A**

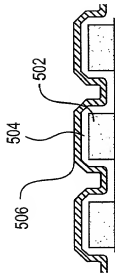


**FIG. 9B**



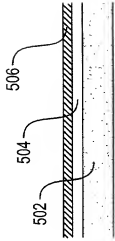
**FIG. 10B**

10015160-1



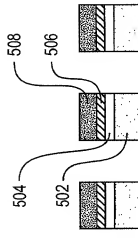
160

**FIG. 11A**



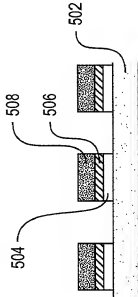
160

**FIG. 11B**



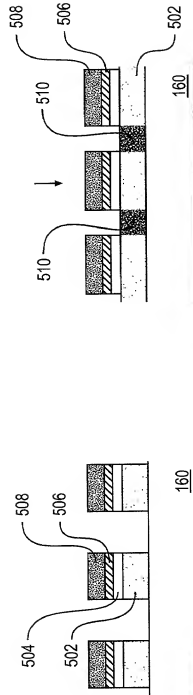
160

**FIG. 12A**

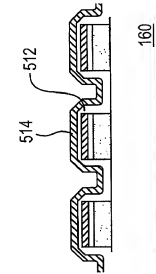


160

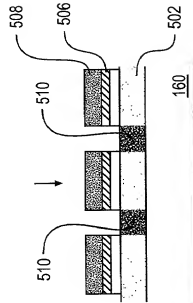
**FIG. 12B**



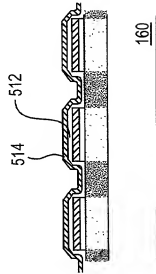
**FIG. 13A**



**FIG. 14A**



**FIG. 13B**



**FIG. 14B**



